REMARKS

Claims 1-15 are pending in the application with claims 1 and 2 amended herein and claims 16-26 cancelled herein. Applicants confirm the provisional election of Invention I, claims 1-15, drawn to a capacitor fabrication method. Applicants herein amended the title to be clearly indicative of the invention as required by the Office Action.

Claims 1, 3-8, and 10-13 stand rejected under 35 USC 102(e) as being anticipated by Chi. Claims 2, 9, 14, and 15 stand rejected under 35 USC 103(a) as being unpatentable over Chi in view of Rhodes. Applicants request reconsideration.

Amended claim 1 sets forth a capacitor fabrication method that includes, among other features, forming a first capacitor electrode comprising TiN over a substrate, forming a capacitor dielectric layer over the first electrode, and forming a second capacitor electrode over the dielectric layer. Claim 1 thus incorporates the subject matter of original claim 2. Pages 3-4 of the Office Action admit that Chi does not disclose a first capacitor electrode comprising TiN. Accordingly, Chi does not anticipate claim 1.

The Office Action relied upon Rhodes for a teaching of a first capacitor electrode comprising TiN and rejected original claim 2 as unpatentable over Chi in view of Rhodes. However, the present application was filed on August 31, 2000 and is thus subject to the provisions of 35 USC 103(c). Rhodes only qualifies as a reference under 35 USC 102(e). Rhodes and the present application are both assigned to Micron Technology, Inc. Accordingly, 103(c) disqualifies Rhodes from use in forming an obviousness rejection. At least for such reason, amended claim 1 is patentable over Chi in view of Rhodes.

Claims 2-9 depend from claim 1 and are further patentable at least for such reason as well as the additional limitations of such claims not disclosed or suggested. For example, claim 8 sets forth that the first electrode is formed by chemisorption of first and second precursors providing a chemisorption product. Chi does not disclose and is not alleged to disclose or suggest such a chemisorption process. Accordingly, the Office Action fails to establish grounds for a rejection of claim 8.

Claim 10 sets forth a capacitor fabrication method that includes, among other features, forming a layer of polysilicon over the sides and bottom of an opening in an insulative layer over a substrate, removing the polysilicon layer from over the bottom, and converting at least some of the polysilicon layer to hemispherical grain polysilicon. The method further includes forming a first capacitor electrode on the converted polysilicon, forming a capacitor dielectric layer on the first electrode, and forming a second capacitor electrode over the dielectric layer. Pages 3-4 of the Office Action allege that Chi discloses the method of claim 10. However, Applicants assert that Chi does not disclose or suggest forming a first capacitor electrode on the "converted polysilicon," as defined in claim 10.

Claim 10 describes that at least some of a polysilicon layer is converted to hemispherical grain polysilicon and the first capacitor electrode is formed on the converted polysilicon. By comparison, column 3, lines 4-19 of Chi clearly describe that the HSG silicon nodules 203 and amorphous silicon sidewall spacers 201 are completely oxidized. That is, nodules 203 and spacers 201 are converted to silicon dioxide. Accordingly, nodules 203 and spacers 201 are no longer HSG silicon of amorphous silicon when the heavily doped polysilicon 301 is formed thereon. Nowhere do s Chi disclose or suggest

that heavily doped polysilicon 301 can be formed on nodules 203 or spacers 201 when such features are still comprised of HSG silicon or amorphous silicon. Anticipation requires disclosure of each and every element of the claimed method. Thus, Chi does not anticipate claim 10. Claim 10 is further not obvious over Chi in view of Rhodes in light of 35 U.S.C. 103(c) as discussed above regarding claim 1.

Claims 11-15 depend from claim 10 and are further patentable at least for such reason as well as the additional limitations of such claims not disclosed or suggested. For example, claim 13 sets forth that the first electrode is formed by chemisorption of first and second precursors providing a chemisorption product. Chi does not disclose and is not alleged to disclose or suggest such a chemisorption process. Accordingly, the Office Action fails to establish grounds for rejection of claim 13. Also for example, claim 14 sets forth that the first electrode comprises TiN. Page 4 of the Office Action admits that Chi does not disclose or suggest TiN as a first electrode. Also, as described above, Rhodes cannot be used in forming an obviousness rejection, accordingly claim 14 is further patentable over the cited art.

All of pending claims 1-15 are herein established as novel and non-obvious over the cited art. Applicants request allowance of such claims in the next Office Action.

Applicants note that a Supplemental Information Disclosure Statement was filed on August 16, 2001 with an accompanying Form PTO-1449. The Office Action Summary of the present Office Action lists PTO-1449 attachments as papers 4, 5, and 6. However, only two of such forms were received. Apparently, paper 5 (filed August 16, 2001) was not attached to the Office Action. Applicants request return of th indicated PTO-1449 with the

Examiner's initials indicating consideration of the listed references either by fax (509-838-3424) to the attention of the undersigned or by inclusion with the next Office Action.

Respectfully submitted,

Dated: 05 Mar 2002 By: _____
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Application Serial No. 09/653,156
Filing Date ..... August 31, 2000
Inventor ..... Vishnu K. Agarwal, et al
Assignee ..... Micron Technology, Inc.
Group Art Unit 2813
Examiner ..... Y. Huynh
Attorney's Docket No. MI22-1518
Title: Capacitor Fabrication Methods and Capacitor Constructions

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO DECEMBER 5, 2001 OFFICE ACTION

In the Specification

The replacement specification paragraphs incorporate the following amendments. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

The title has been amended as follows:

Capacitor Fabrication Methods ~~and Capacitor Constructions~~

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

1. (once amended) A capacitor fabrication method comprising:

forming a first capacitor electrode comprising TiN over a substrate, the first electrode having an inner surface area per unit area and an outer surface area per unit area that are both greater than an outer surface area per unit area of the substrate;

forming a capacitor dielectric layer over the first electrode; and

forming a second capacitor electrode over the dielectric layer.

2. (once amended) The method of claim 1 wherein the first electrode ~~comprises~~ consists of TiN.

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